REMARKS/ARGUMENTS

This Amendment is in response to the Office Action dated April 9, 2003, the deadline to which has been extended by three (3) months from July 9, 2003 to October 9, 2003, by petition and payment of fee. Claims 1-22 are pending in the present application. Claims 9-22 have been rejected. Claims 1-8 have been withdrawn from consideration. Accordingly, claims 9-22 are pending. For the reasons set forth more fully below, Applicant respectfully submits that the claims as presented are allowable. Consequently, reconsideration, allowance, and passage to issue are respectfully requested.

Claim Rejections – 35 U.S.C. 103

The Examiner has stated,

> **Claims 9-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ellul et al. in view of Thomas et al.**
>
> **Regarding claim 9, Ellul et al. (US 5,614,750) teaches a semiconductor device (Figure 6) comprising a substrate 52, a plurality of device structures 90, a buried layer 54, an interconnect comprising a slot 78, a conductive material 82 in the slot, oxidized sidewalls 80 which forms a sinker to the buried layer (column 4, lines 63-67). Thomas et al. (US 4,933,743) teaches a metal 26 in a slot to form an interconnect. It would have been obvious to one of ordinary skill in the art to use a metal in the device of Ellul et al. since Ellul et al. teaches the use of other conductive materials such as those taught by Thomas et al.**
>
> **Regarding claims 10-12, Thomas et al. further teaches multiple metals in the interconnect slot which partially fill the slot with a final metal which provides the interconnect layer. It would have been obvious to one of ordinary skill in the art to use the multiple metals of Thomas et al. in the device Ellul et al. since the structure of Thomas et al. provides lower resistance and improved electromigration resistance (column 2, lines 63-67).**
>
> **Regarding claim 17, Ellul et al. further teaches a sinker coupled to a collector 55.**
>
> **7. Regarding claim 13, Ellul et al. teaches a semiconductor device (Figure 6) comprising a buried layer 54, an interconnect comprising a slot 78, a conductive material 82 in the slot, oxidized sidewalls 80 which forms a sinker to**

the buried layer (column 4, lines 63-67). Thomas et al. teaches a metal 26 in a slot to form an interconnect. It would have been obvious to one of ordinary skill in the art to use a metal in the device of Ellul et al. since Ellul et al. teaches the use of other conductive materials such as those taught by Thomas et al.

Regarding claims 14-16, 20, and 22, Thomas et al. further teaches multiple metals in the interconnect slot which partially fill the slot with a final metal which provides the interconnect layer where the high current carrying conductors are on the same level (Figure 1L). It would have been obvious to one of ordinary skill in the art to use the multiple metals of Thomas et al. in the device Ellul et al. since the structure of Thomas et al. provides lower resistance and improved electromigration resistance (column 2, lines 63-67).

Regarding claim 18, Ellul et al. further teaches a slot coupled to the emitter 94.

Regarding claims 19 and 21, Ellul et al. further teaches a CMOS integrated circuit structure with a bipolar device. Thomas et al. teaches an integrated circuit with bipolar and MOS logic circuits on the same device (column 1, lines 12-25). It would have been obvious to one of ordinary skill in the art to use the device of Ellul et al. in an IC comprising bipolar transistors and MOS transistors since these are well known in the art as devices integrated on the same circuit using high voltage interconnects.

Applicant respectfully disagrees.

Claim 9 and 13 are reproduced in its entirety hereinbelow:

9. A semiconductor device comprising:

a semiconductor substrate, the semiconductor substrate including a plurality of device structures thereon, and a buried layer in the semiconductor substrate; and

an interconnect on the semiconductor substrate, the interconnect comprising at least one slot provided in the semiconductor substrate and at least one metal within the slot, wherein the at least one slot is oxidized everywhere except at the bottom of the slot, and the interconnect forms a sinker to the buried layer.

13. A high voltage interconnect on a semiconductor substrate, the substrate including a buried layer comprising:

a slot provided in the semiconductor substrate; and

at least one metal within the slot, wherein the at least one slot is oxidized everywhere except at the bottom of the slot, and the interconnect forms a sinker to the buried layer.

DISCUSSION

As is recited in the claims, in the interconnect of the present invention includes "at least one slot . . . and at least one metal in the slot." referring to column 4, lines 58-61 of Ellul," The trench is lined with dielectric spacers 80, and filled with a conductive layer 82. "The conductive layer 82 comprising heavily doped polysilicon" emphasis added. Providing polysilicon with a slot is clearly different from providing a metal within the slot. The metal within the slot allows for high power, high current operation of semiconductor device. Ellul neither teaches nor suggests such an operation. Thomas although describing an interconnect neither teaches nor suggests the interconnect of the recited invention. Accordingly, Applicant submits that claims 9-22 are allowable over the cited references.

Accordingly, Applicant's attorney believes that this application is in condition for allowance. Should any unresolved issues remain, Examiner is invited to call Applicant's attorney at the telephone number indicated below.

Respectfully submitted,
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